ARES: Abstract Representations for the Extreme-Scale Stack

- Create a universal high-level intermediate representation
  - HLIR defined that includes heterogeneous computing and complex memory hierarchy concepts
- Develop prototype frontends
  - OpenACC and OpenMP offload frontends developed and deployed
- Develop prototype optimization engine for HLIR
  - Optimization engine recognizes and optimizes
- Develop back-end compilation, based on LLVM
  - HLIR lowered to LLVM IR, gaining benefits of LLVM infrastructure
- Demonstrate HLIR benefits on application examples
  - IMPACC, NVL-C, OpenACC2FPGA, FITL, etc