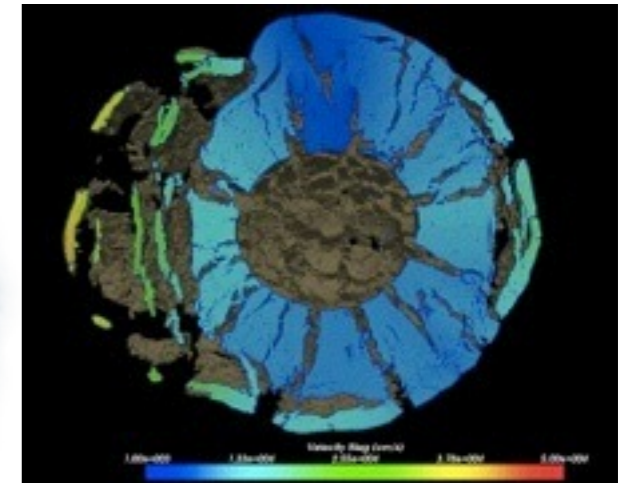
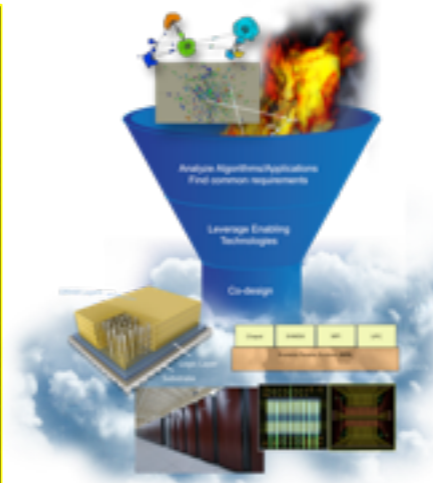
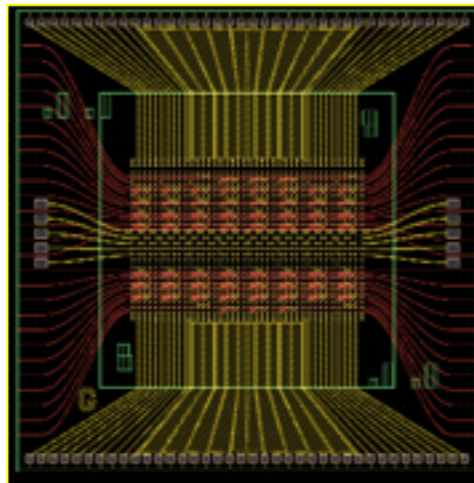
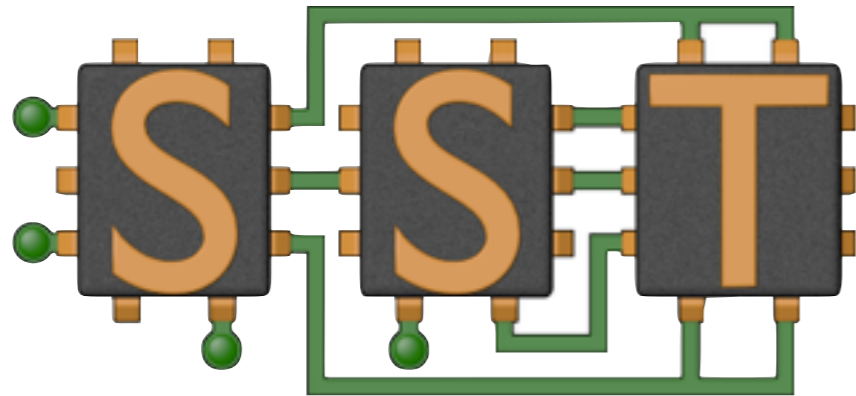


Exceptional service in the national interest



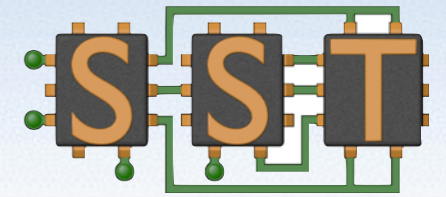
The Structural Simulation Toolkit (SST)

Arun Rodrigues



Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. SAND NO. 2011-XXXXP

SST Simulation Project Overview



Goals

- Become the standard architectural simulation framework for HPC
- Be able to evaluate future systems on DOE/DOD workloads
- Use supercomputers to design supercomputers

Status

- Parallel Core, basic components
- Current Release (3.1)
 - Improved set of components
 - Improved portability

Technical Approach

- Parallel
 - Parallel Discrete Event core with conservative optimization over MPI
- Multiscale
 - Detailed and simple models for processor, network, and memory
- Interoperability
 - gem5, DRAMSim, cache models
 - routers, NICs, schedulers, GPGPU
- Open
 - Open Core, non viral, modular

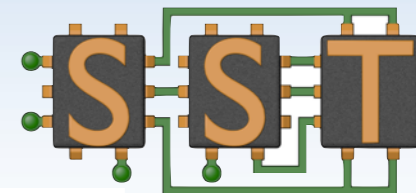


Consortium

- “Best of Breed” simulation suite
- Combine Lab, academic, & industry

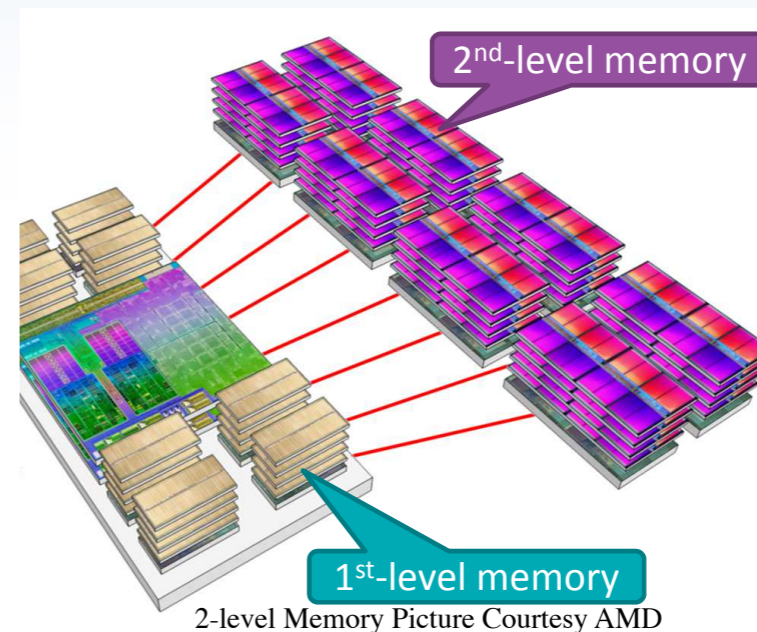


SST Capabilities



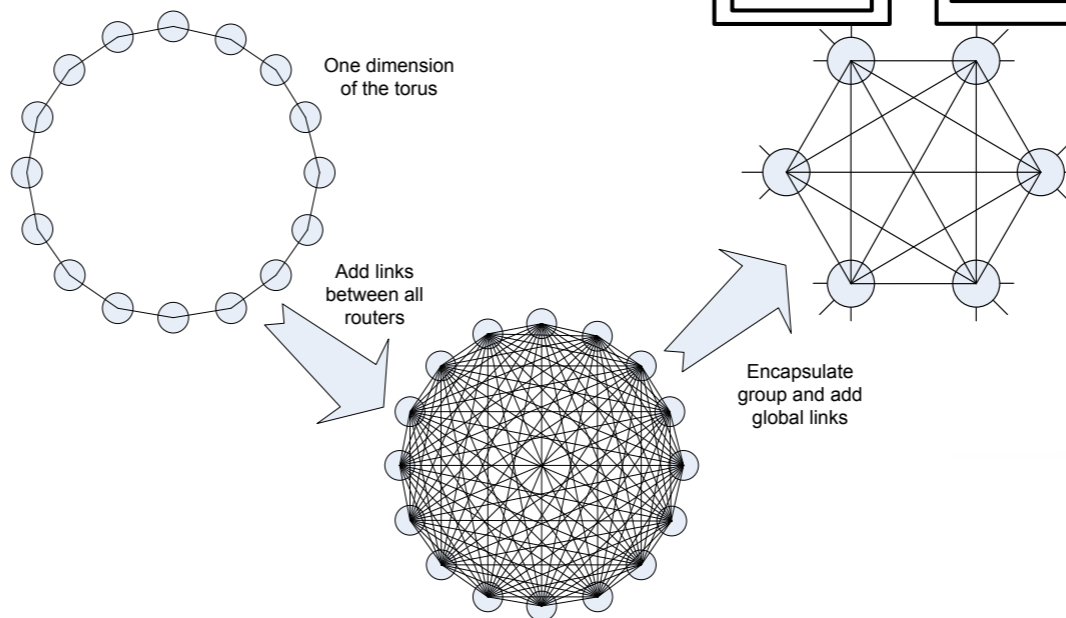
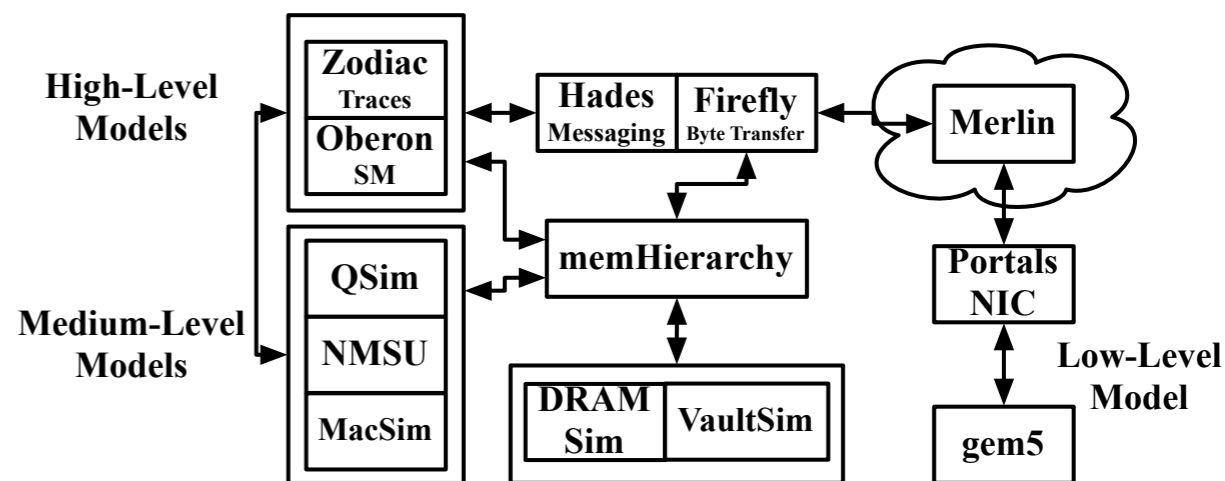
• Memory Simulations

- Extensive cache models
 - Snoopy and Directory-based coherency models
 - Multiple pre-fetcher models
- Multiple Drivers
 - Execution driven (gem5, pintool, qsim)
 - Trace driven (ariel, oberon)
- Accurate Memory Simulators
 - DRAMSim, VaultSim, HybridSim



• Network Simulations

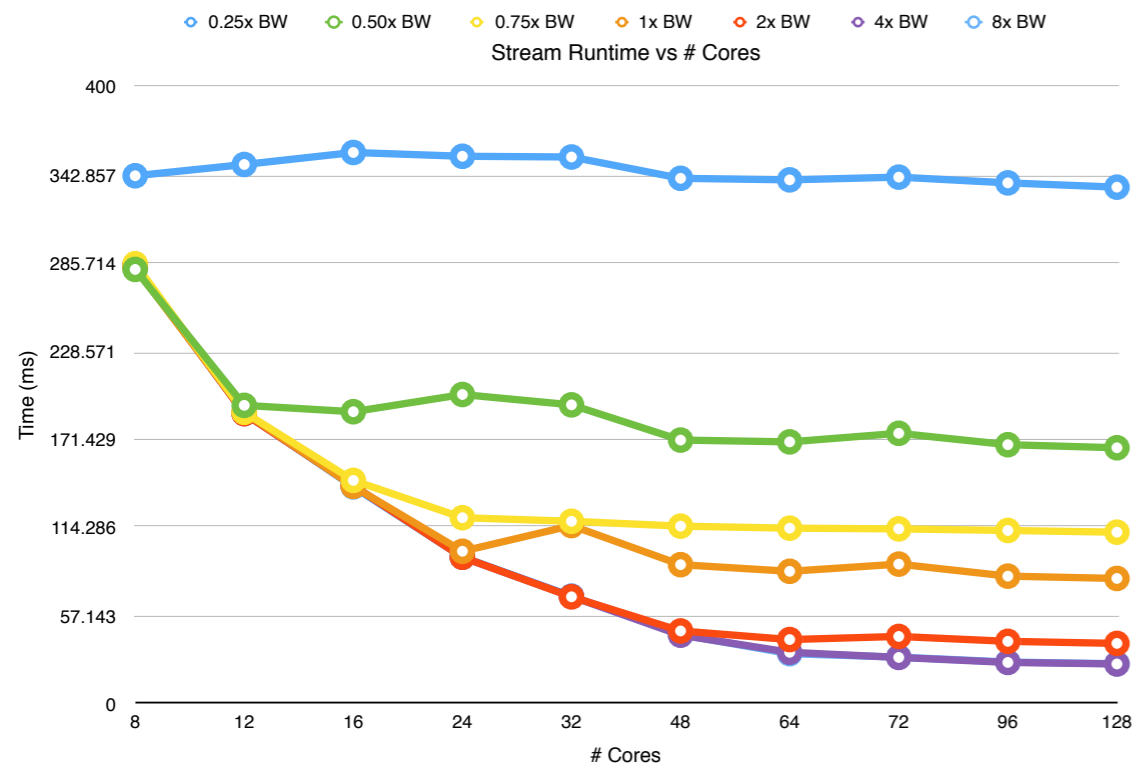
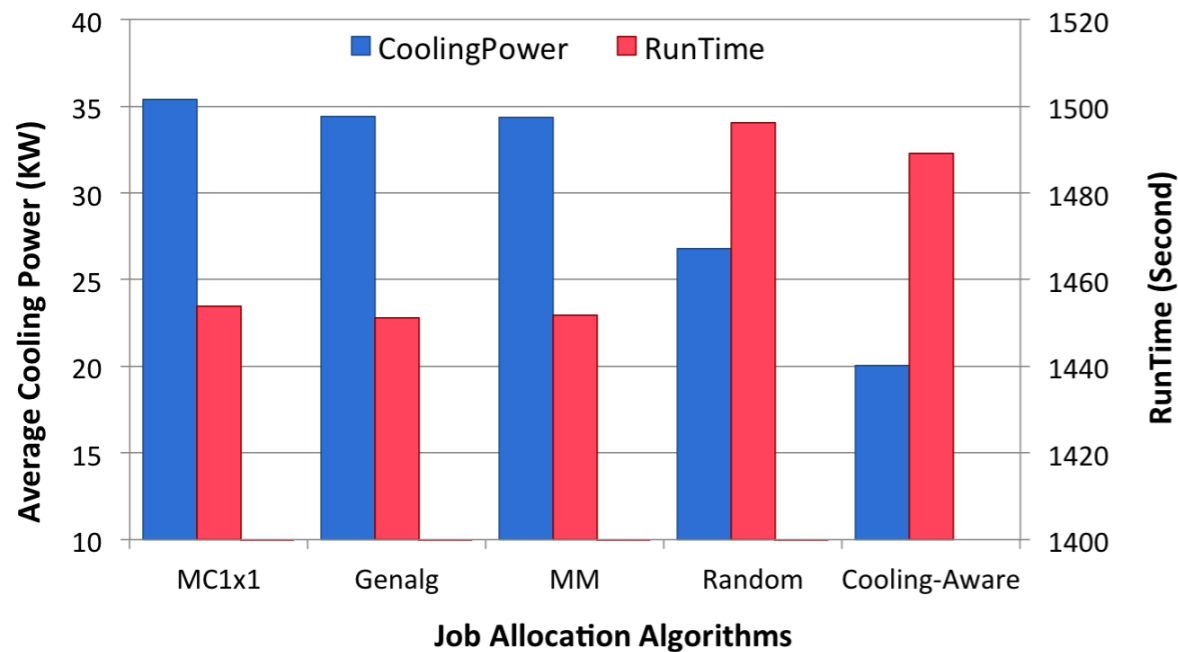
- High-performance network topologies
 - N-dim Torus, Fat-tree, Dragonfly, etc.
- Multi-scale
 - Network-on-chip
 - 100K+ nodes
- Multiple Drivers
 - Traces
 - State-machines
 - Pattern-based stochastic



• System-level Simulations

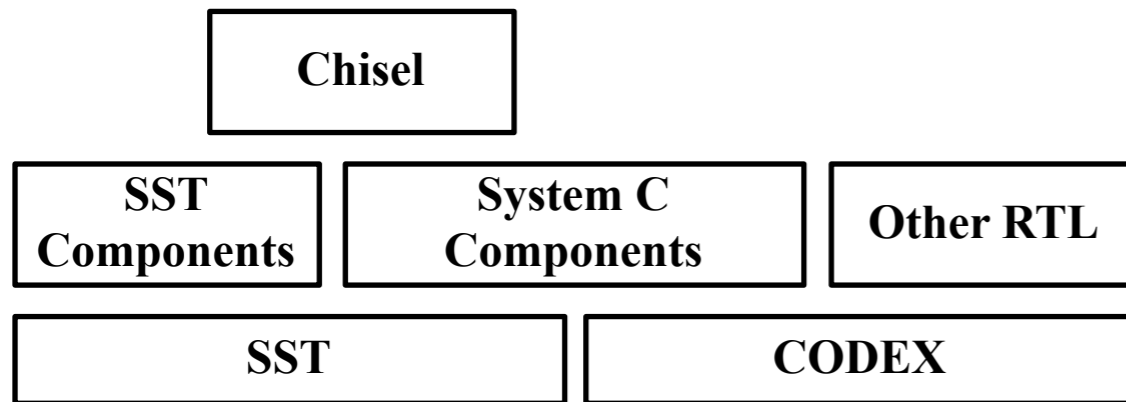
- Job scheduling & Allocation

SST Recent Results



- Examined different Job allocation algorithms
- Geometry-, cooling-, and power- aware allocation algorithms
- Timescale: Months
- Memory Benchmarks
 - STREAMS benchmark to indicate we are getting correct memory BW
 - Memory contention curves match real systems
 - Timescale: Seconds

Interconnections



- SST is generic framework
- Supports many other simulators
- Planned reuse of Chisel & System C components w/ CODEX
- Planned integration with “SST/Macro” components

