Traleika Glacier (X-Stack) – Intel Team

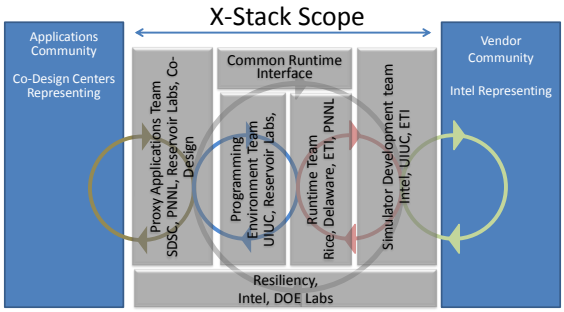
Goals and Objectives

Goal:
Research and mature software technologies addressing major Exascale challenges and get ready to intercept by 2018-2020

Objectives:

Energy efficiency	SW components interoperate, harmonize, exploit HW features, and optimize the system for energy efficiency
Data locality	PGM system & system SW optimize to reduce data movement
Scalability	SW components scalable, portable to $O(10^9)$—extreme parallelism
Programmability	New (Codelet) & legacy (MPI), with gentle slope for productivity
Execution model	Objective function based, dynamic, global system optimization
Self-awareness	Dynamically respond to changing conditions and demands
Resiliency	Asymptotically provide reliability of N-modular redundancy using HW/SW co-design; HW detection, SW correction

Scope of Traleika Glacier Project



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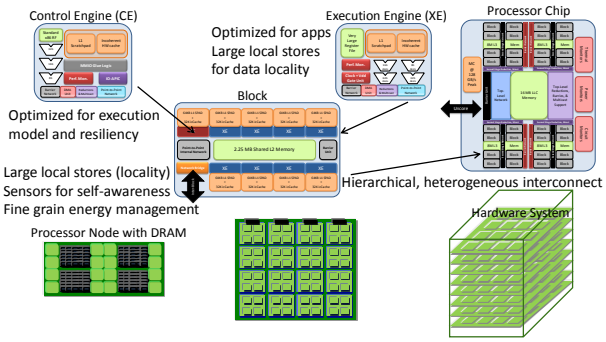
Straw-man System Architecture and Evaluation



Architecture embraces data-locality, and tapered BW

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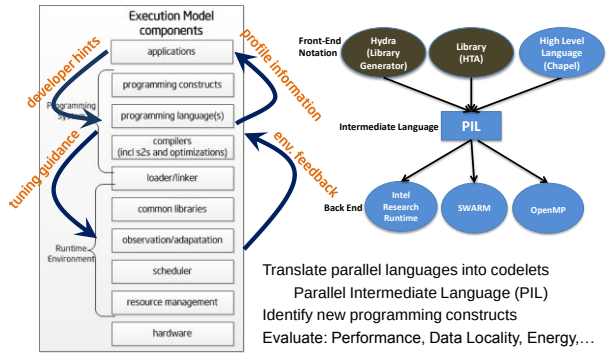
Programming System Components



Translate parallel languages into codelets
Parallel Intermediate Language (PIL)
Identify new programming constructs
Evaluate: Performance, Data Locality, Energy,…

Runtime Research Agenda

- **Locality aware scheduling—heuristics for locality/E-efficiency**
  - Extensions to standard Habanero-C runtime
- **Adaptive boosting and idling of hardware**
  - Avoid energy expensive unsuccessful steals that perform no work
  - Turbo mode for a core executing serial code
  - Fine grain resource (including energy) management
- **Dynamic data-block movement**
  - Co-locate codelets and data
  - Move codelets to data
- **Introspection and dynamic optimization**
  - Performance counters, sensors provide real time information
  - Optimization of the system for user defined objective
  - (Go beyond energy proportional computing)

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Simulators and Tools, Leverage UHPC, and Go Beyond

Simulator	Pros	Cons
AFL Application faking Library IRR API + Extensions	• 64-bit Linux IRR implementation • Near-native application code execution on host processor • Rapid application development • Epoch statistics as well as total statistics	• Does not model real architecture • Does not model advanced ISA features • Does not reflect expected timing of simulated system
FSim Functional Simulator	• Every hardware unit modeled, exact memory and network hierarchies including messages • Complete statistics and trace file • >10 MIPS per core speed • Massively parallel and distributed, limited only by machine pool	• Does not have a timing model • Lower speed, highly detailed

Tool	Purpose	Advantage	Weakness
Power Estimator	• Uses statistics/counters to make energy and area estimates for application behavior	• Scales from 45nm to 7nm projections • Automatic analysis of outputs from FSim runs	• Only models dynamic power, uses circuit models for leakage • Calibrated to existing commercial devices
Memory Analyzer	• Detailed models for cache and/or scratchpad hierarchies, various levels & types of coherence • Compares configurations	• Calls into Power Estimator • Enables limited AFL trace power estimation	• Does not model Instruction fetch/execution • Limited to AFL-compatible memory traces at this time

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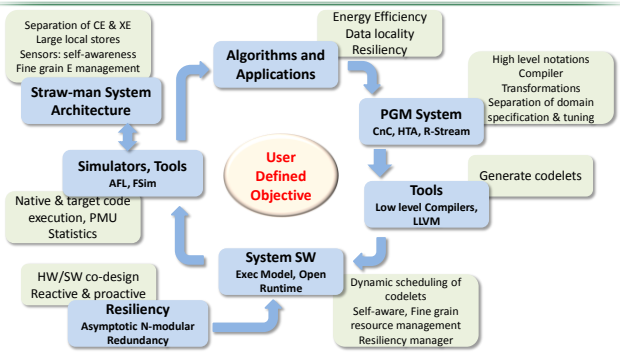
X-Stack Components Put Together



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3 Year Roadmap

	2012	2013				2014				2015		
	Q4'12	Q1'13	Q2'13	Q3'13	Q4'13	Q1'14	Q2'14	Q3'14	Q4'14	Q1'15	Q2'15	Q3'15
Algorithms and applications												
Proxy app evaluation for O(compute)	<----------	----------	----------	----------	---------->							
Proxy app evaluation for O(comm)			<----------	----------	---------->							
Evaluation of system architecture						-----	V2.0	----------	----------	-----	V2.5	----------	----------	-----	V3.0>
Programming system												
Select apps coded, for runtime system	<----------	----------	----------	-----	V2.0-	----------	----------	----------	-----	V2.5	----------	----------	-----	V3.0>
Tools	<C+binuti	ls-V2.0-->	<----------	De	bugger-->	----------	----------	-----	V2.5	----------	----------	-----	V3.0	----------	----------	-----
Resiliency	<---Frame	work-----	---->	<-----Reac	tive------>	<---Reco	very---->	<-----Proac	tive----->	<----------	Evaluate	Validate	---------->			
Execution Model, Sys SW, Runtime	<-- Mod fo	r IRR----->	<-Intelligi nt Sched->	<-Eval-----		V2.0	----------	----------	V2.5	----------	----------	-----	OCR	-----	V3.0>
Architecture, simulators	<A V2.0>	<Sim2.0>	<Fault M>	<Timing>	<-Eval-->	<A V2.5>	<Sim 2.5>	<-Eval-->	<A V3.0>	<Sim 3.0>	<-----Eval uate----->				
System Evaluation	<----------	----------	----------	----------	For 2.5--->			For 3.0--->		----------	----------	----------	----------	----------	---------->

Arch Rev 1 (UHPC leveraged)
Arch Rev 2 incorporates X-Stack
Arch Rev 2.5 enhanced for X-Stack with initial findings
Arch Rev 3.0 X-Stack final
Final Evaluation Release OCR 1.0

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